REMARKS

Claims 1-4 have been examined on their merits.

Applicant herein amends claims 1-4 to more clearly recite that the logic operation information for a circuit represents correspondence between logical state transitions at an output terminal due to logical state transitions at an input terminal. The delay information is based upon the types of logical state transitions at the input and output terminals. Support for the amendments to claims 1-4 can be found at, for example, pages 3, lines 2-9; page 4, line 23 to page 5, line 8; page 5, line 24 to page 6, line 18 and Figures 1(a) to 1(c). No new matter has been added. Entry and consideration of the amendments to claims 1-4 is respectfully requested.

Claim 1-4 are all the claims presently pending in the application.

1. Claims 1-4 stand rejected under 35 U.S.C. § 112 (1st para.) as allegedly containing subject matter that was not described in the specification in such a way as to reasonably convey that the inventor was in possession of the claimed invention. Applicant respectfully traverses the rejection of claims 1-4 for at least the reasons discussed below.

An applicant shows possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention. *Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572 (Fed. Cir. 1997). The subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to

satisfy the description requirement. MPEP § 2163.02. A description as filed is presumed to be adequate, unless sufficient evidence or reasoning to the contrary has been presented by the examiner to rebut the presumption. *In re Marzocchi*, 439 F.2d 220, 224 (CCPA 1971). The examiner must have a reasonable basis to challenge the adequacy of the written description, and must show by a preponderance of evidence why a person skilled in the art would not recognize in an applicant's disclosure a description of the invention defined by the claims. *In re Wertheim*, 541 F.2d 257, 262, 263 (CCPA 1976). For the reasons below, the Examiner has not met the burden imposed by *Wertheim.*

For claims 1-4, the Examiner argues that the "specification does not describe anywhere the delay information being stored in the library based upon the logical state represented by the logical operation information." The present invention references a delay analysis library to select a delay time of logic circuit. *See* page 5, lines 9-12. In an exemplary non-limiting embodiment, a delay analysis library, which includes delay information, is described on page 6, lines 5-18 in conjunction with Figures 1(a) and 1(b). Figure 1(a) is an AND gate, and the delay information is based on the logical state transitions at the input terminals and the output terminal of the AND gate. Applicant assumes that one of even rudimentary skill in the art understands how an AND gate operates, and moreover, it is not necessary to describe the AND gate's operation. A patent need not teach, and preferably omits, what is well known in the art. *In re Buchner*, 929 F.2d 660, 661 (Fed. Cir. 1991).

For claims 1-4, the Examiner argues that the "specification does not describe anywhere how the logical state is derived from the logical operation information and what the logical state is." As noted above, in an exemplary non-limiting embodiment, a delay analysis library, which includes delay information, is described on page 6, lines 5-18 in conjunction with Figures 1(a) and 1(b). Figure 1(a) is an AND gate, and the delay information is based on the logical state transitions at the input terminals and the output terminal of the AND gate. For example, in the first line of Figure 1(b), an input pin (Terminal 1) and the output pin (Terminal 3) of the AND gate shown in Figure (1) are listed. The first line further illustrates that if the logic state of the input pin rises, then the logic state of the output pin rises as well, with a 1 nanosecond time delay. See page 6, lines 4-20. Applicant assumes that one of even rudimentary skill in the art understands that if the logical state of one input of an AND gate rises, causing the logical state of the output terminal to rise, then all the other remaining input pins of the AND must have high logical states as well. Again, a patent need not teach, and preferably omits, what is well known in the art. *In re Buchner*, 929 F.2d 660, 661 (Fed. Cir. 1991).

For claims 1-4, the Examiner argues that the "specification does not describe what the current logical state is and how it is different from the logical state as represented by said logical operation information for said at least one circuit." This argument is now moot since claims 1-4 no longer recite this limitation.

Thus, based on the foregoing reasons, Applicant requests that the Examiner withdraw the 35 U.S.C. § 112 (1st para.) rejection of claims 1-4. If the Examiner persists in maintaining the 35

U.S.C. § 112 (1st para.) rejection of claims 1-4, Applicant requests that the Examiner comply with the requirements for making a proper 35 U.S.C. § 112 (1st para.) rejection as listed in the MPEP and reproduced above.

2. Claims 1-4 stand rejected under 35 U.S.C. § 112 (2nd para.) as allegedly being indefinite. Applicant respectfully traverses the rejection of claims 1-4 for at least the reasons discussed below.

If the examiner makes a rejection under 35 U.S.C. § 112 (2nd para.), an analysis as to why the phrases used in the rejected claim is "vague and indefinite" should be made. The examiner should make the record clear by providing explicit reasoning for making any rejection related to 35 U.S.C. 112, second paragraph. *See* MPEP § 2173.02. In the November 20, 2003 Non-Final Office Action, the Examiner has ignored these requirements for a proper rejection under 35 U.S.C. § 112 (2nd para.). Nevertheless, Applicant will show that the Examiner's 35 U.S.C. § 112 (2nd para.) rejection is unsupportable.

For claims 1-4, the Examiner states that the system means for storing delay information in the library is vague and indefinite. The specification states that "delay time information on the rise and fall of input and output pins, such as that shown in FIG. 1(b), is contained also in the conventional delay analysis library." *See* page 6, lines 15-18.

For claims 1-4, the Examiner states that the system means for selecting the delay time from the delay information is vague and indefinite. The specification states that the delay

analysis system can be implemented by a computer executable code. It would be understood by one of ordinary skill in the art that such a delay analysis system would be implemented on a computer system. Furthermore, page 7, line 10 through page 8, line 15, along with Figures 3 and 4, disclose how a delay time is selected from the delay information.

Thus, based on the foregoing reasons, Applicant requests that the Examiner withdraw the 35 U.S.C. § 112 (2nd para.) rejection of claims 1-4. However, f the Examiner persists in maintaining the 35 U.S.C. § 112 (2nd para.) rejection of claims 1-4, Applicant requests that the Examiner comply with the requirements for making a proper 35 U.S.C. § 112 (2nd para.) rejection as listed in the MPEP and reproduced above.

3. Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Blinne *et al.* (U.S. Patent No. 5,274,568) in view of Hasegawa (U.S. Patent No. 6,041,168) (hereinafter Hasegawa '168) and in further view of Hasegawa (U.S. Patent No. 5,528,511) (hereinafter Hasegawa '511). Applicant traverses the rejection of claims 1-4 for at least the reasons discussed below.

The Examiner acknowledges that Blinne *et al.* fail to teach or suggest that, for at least one of a plurality of circuits, a library that comprises logical operation information. *See* November 20, 2003 Non-Final Office Action, page 12. The Examiner alleges that Hasegawa '168 supplies the necessary disclosure to overcome the acknowledged deficiencies of Blinne *et al.*

The Examiner acknowledges that the combination of Blinne *et al.* and Hasegawa '168 fail to teach or suggest logical operation information representing correspondence between a logical value of each input terminal and the logical value of the output terminal of at least one of a plurality of circuits. *See* November 20, 2003 Non-Final Office Action, page 13. The Examiner alleges that Hasegawa '511 supplies the necessary disclosure to overcome the acknowledged deficiencies of the combination of Blinne *et al.* and Hasegawa '168.

Hasegawa '511 discloses, *inter alia*, a delay time verification method that provides propagation delay times even when the rising edge or the falling edge of a signal is meaningless. *See* col. 2, lines 63-65 of Hasegawa '511. The method disclosed by Hasegawa '511 uses nodes and arcs in a fashion similar to Hasegawa '168. *See, e.g.*, col. 5, lines 16-23 of Hasegawa '511.

With respect to claim 1, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to teach or suggest a delay analysis library comprising delay information for a circuit that is based upon the logical state transitions at the input and output terminals of a logical circuit, where the analysis library stores the delay information based on the correspondence between the input terminal logical state transitions and the output terminal logical state transitions. The combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 does not use input terminal logical state transitions, output terminal logical state transitions and delay information in the same manner as the present invention. In the present invention, delay times are based upon the current logical state of a logic circuit, and the types of state transitions that are present on the input and output terminals of the logic circuit. A rising edge signal might have

two different propagation delay times, based on the logical state of the circuit and the logical states of the other input signals. On the other hand, Blinne *et al.* are concerned with the propagation time of a rising or falling edge through a logic cell. *See* col. 1, lines 45-48 of Blinne *et al.* Blinne *et al.* do not teach or suggest determining delay time based on the current logical state of a circuit and how the input signal transitions will affect that logical state. Blinne *et al.* ignore the logic operation of the analyzed logic circuit by independently recording each of the many inputs of the logic circuit. Inputs not being measured are fixed to a predetermined logic level while measuring the delay time of the remaining input. *See, e.g.*, col. 8, lines 33-39; Fig. 1 of Blinne *et al.* In calculating the maximum delay time for the logic circuit, Blinne *et al.* uses the delay time of the input with the longest delay time. For example, this delay time is longer than what would be found in normal AND gate operation, because in that case the output falls as soon as the input with the shortest delay time falls. Hasegawa '168 does not even disclose signal transitions, but instead adds a series of maximum delay times together to determine a propagation delay. *See* col. 5, lines 23-34; Fig. 5 of Hasegawa '168. While the circuit modeling technique disclosed by Hasegawa '511 uses rising and falling signals, Hasegawa '511 still rely upon maximum delay times, stored in the arcs between nodes, for propagation delay time calculations. *See* col. 6, lines 54-56 of Hasegawa '511. Hasegawa '511 does not teach or suggest determining delay time based on the logical state transitions at the input and output terminals. The combining of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 with each other does not remove this fundamental deficiency which permeates each of the references. In the

three references, the propagation delay time for a logic circuit is arrived at using maximum delay times, and there is no discussion of using the input signal transitions and the current logical state of the logic circuit as index to a propagation delay time that is representative of how the logic circuit actually operates.

In addition, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to teach or suggest that a delay time is selected from delay time information according to input terminal and output terminal logical state transitions, as recited in claim 1. The Examiner acknowledges that Blinne *et al.* fail to teach or suggest this feature of the present invention.[1] The Examiner alleges that Hasegawa '511 provides the necessary disclosure to overcome the acknowledged deficiencies of Blinne *et al.* As discussed above, Hasegawa '511 does not teach or suggest determining delay time based on the current logical state of a circuit and the logical state transitions at the input and output terminals. Instead, Hasegawa '511 uses the maximum delay time between two nodes in performing its delay calculations, so that rising edge signals and falling edge signals use the same estimated delay time for delay calculations. Unlike the present invention, Hasegawa '511 does not differentiate between the type of signal transition at the input of a logic circuit when determining a delay time, and Hasegawa '511 does not use the type of logical state transitions present at both the input and output terminals of a logic circuit when selecting a delay time for a particular signal propagation through the logic circuit.

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[1] It is clear that Hasegawa '168 fails to teach or suggest this feature of the invention as well, since the analysis method disclosed in Hasegawa '168 does not involve signal transitions or the logical operation of the modeled circuit.

Thus, Applicant believes that the Examiner cannot fulfill the "all limitations" prong of a *prima facie* case of obviousness with respect to claim 1, as required by *In re Vaeck*.

Since Blinne *et al.*, Hasegawa '168 and Hasegawa '511 do not disclose a delay analysis library comprising delay information for a circuit that is based upon the type of signal transitions present at the circuit's input and output terminals as represented by stored logical operation information, Applicant believes that one of skill in the art would not be motivated to combine the three references. Although the Examiner provides a generalized motivation analysis with respect to a delay analysis method, none of the references disclose providing delay information for a circuit that is based upon the type of signal transitions present at the circuit's input and output terminals as represented by stored logical operation information. As discussed above, Blinne *et al.*, Hasegawa '168 and Hasegawa '511 rely on using the maximum delay time that is stored for a particular logic circuit when that particular logic circuit is undergoing propagation delay analysis. *See, e.g.*, col. 8, lines 33-39; Fig. 1 of Blinne *et al.*; col. 5, lines 23-34; Fig. 5 of Hasegawa '168; col. 6, lines 54-56 of Hasegawa '511. In addition, none of the references teach or suggest that a delay time is selected from delay time information according to the type of logical state transitions present at both the input and output terminals of a circuit, as recited in claim 1. Since none of the references teach or suggest these features of claim 1, Applicant submits that one of ordinary skill in the art would not have been motivated to combine the three references. Thus, Applicant believes that the Examiner cannot fulfill the motivation prong of a

prima facie case of obviousness with respect to claim 1, as required by *In re Dembiczak* and *In re Zurko*.

Based on the foregoing reasons, Applicant believes that the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to disclose all of the claimed elements as arranged in claim 1. Therefore, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 clearly cannot render the present invention obvious as recited in claim 1. Thus, Applicant believes that claim 1 is in condition for allowance. Applicant respectfully requests that the Examiner withdraw the § 103(a) rejection of claim 1.

With respect to claim 2, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to teach or suggest a delay analysis library comprising delay information for a circuit that is based upon the type of logical state transitions present at the circuit's input and output terminals as represented by stored logical operation information. As discussed above with respect to claim 1, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 does not use the type of logical state transitions at both the input and output terminals of a circuit in the same manner as the present invention. In addition, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to teach or suggest selecting a delay time between an input terminal and an output terminal of a logic circuit from stored delay time information according to the type of logical state transitions for the input and output terminals. The Examiner

acknowledges that Blinne *et al.* fail to teach or suggest this feature of the present invention.[2] The Examiner alleges that Hasegawa '511 provides the necessary disclosure to overcome the acknowledged deficiencies of Blinne *et al.* As discussed above with respect to claim 1, Hasegawa '511 does not teach or suggest determining delay time based on the type of logical state transitions present at both the input and output terminals of a logic circuit. Instead, Hasegawa '511 uses the maximum delay time between two nodes in performing its delay calculations, so that rising edge signals and falling edge signals use the same estimated delay time for delay calculations. Unlike the present invention, Hasegawa '511 does not differentiate between the type of signal transition at the input of a logic circuit when determining a delay time, and Hasegawa '511 does not use the type of logical state transitions for the input and output terminals when selecting a delay time for a particular signal propagation through the logic circuit.

Thus, Applicant believes that the Examiner cannot fulfill the "all limitations" prong of a *prima facie* case of obviousness with respect to claim 2, as required by *In re Vaeck*.

Since Blinne *et al.*, Hasegawa '168 and Hasegawa '511 do not disclose a delay analysis library comprising delay information for a circuit that is based upon the type of logical state transitions for the input and output terminals as represented by stored logical operation information, Applicant believes that one of skill in the art would not be motivated to combine the

[2] It is clear that Hasegawa '168 fails to teach or suggest this feature of the invention as well, since the analysis method disclosed in Hasegawa '168 does not involve signal transitions or the logical operation of the modeled circuit.

three references. None of the references disclose providing delay information for a circuit that is based upon the type of logical state transitions for the input and output terminals as represented by stored logical operation information. As discussed above with respect to claim 1, Blinne *et al.*, Hasegawa '168 and Hasegawa '511 rely on using the maximum delay time that is stored for a particular logic circuit when that particular logic circuit is undergoing propagation delay analysis. *See, e.g.*, col. 8, lines 33-39; Fig. 1 of Blinne *et al.*; col. 5, lines 23-34; Fig. 5 of Hasegawa '168; col. 6, lines 54-56 of Hasegawa '511. In addition, none of the references teach or suggest selecting a delay time between an input terminal and an output terminal of a logic circuit from stored delay time information according to the type of logical state transition present at the input and output terminals, as recited in claim 2. Since none of the references teach or suggest these features of claim 2, Applicant submits that one of ordinary skill in the art would not have been motivated to combine the three references. Thus, Applicant believes that the Examiner cannot fulfill the motivation prong of a *prima facie* case of obviousness with respect to claim 2, as required by *In re Dembiczak* and *In re Zurko*.

Based on the foregoing reasons, Applicant believes that the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to disclose all of the claimed elements as arranged in claim 2. Therefore, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 clearly cannot render the present invention obvious as recited in claim 2. Thus, Applicant believes that claim 2 is in condition for allowance. Applicant respectfully requests that the Examiner withdraw the § 103(a) rejection of claim 2.

With respect to claims 3 and 4, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to teach or suggest referencing a delay analysis library comprising delay information for a circuit that is based upon the type of logical state transitions for the input and output terminals as represented by stored logical operation information. As discussed above with respect to claim 1, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 does not reference a delay analysis library comprising the types of logical state transitions at input and output terminals that correspond to delay times in the same manner as the present invention. In addition, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to teach or suggest selecting a delay time based on the type of logical state transitions present at the input and output terminals of a logical circuit, as recited in claims 3 and 4. The Examiner acknowledges that Blinne *et al.* fail to teach or suggest this feature of the present invention.[3] *See* June 16, 2003 Final Office Action, pages 8 and 10, respectively. The Examiner alleges that Hasegawa '511 provides the necessary disclosure to overcome the acknowledged deficiencies of Blinne *et al.* As discussed above with respect to claim 1, Hasegawa '511 does not teach or suggest determining delay time based on the type of logical state transitions present at the input and output terminals of a logical circuit. Instead, Hasegawa '511 uses the maximum delay time between two nodes in performing its delay calculations, so that rising edge signals and falling edge signals use the same estimated delay time for delay calculations. Unlike the present

[3] It is clear that Hasegawa '168 fails to teach or suggest this feature of the invention as well, since the analysis method disclosed in Hasegawa '168 does not involve signal transitions or the logical operation of the modeled circuit.

invention, Hasegawa '511 does not differentiate between the type of signal transition at the input of a logic circuit when determining a delay time, and Hasegawa '511 does not use the logical state transitions present at both the input and output terminals when selecting a delay time for a particular signal propagation through the logic circuit.

Thus, Applicant believes that the Examiner cannot fulfill the "all limitations" prong of a *prima facie* case of obviousness with respect to claims 3 and 4, as required by *In re Vaeck.*

Since Blinne *et al.*, Hasegawa '168 and Hasegawa '511 do not disclose a delay analysis library comprising delay information for a circuit that is based upon the type of logical state transitions present at a circuit's input and output terminals as represented by stored logical operation information, Applicant believes that one of skill in the art would not be motivated to combine the three references. None of the references disclose providing delay information for a circuit that is based upon the type of logical state transitions present at the circuit's input and output terminals as represented by stored logical operation information. As discussed above with respect to claim 1, Blinne *et al.*, Hasegawa '168 and Hasegawa '511 rely on using the maximum delay time that is stored for a particular logic circuit when that particular logic circuit is undergoing propagation delay analysis. *See, e.g.*, col. 8, lines 33-39; Fig. 1 of Blinne *et al.*; col. 5, lines 23-34; Fig. 5 of Hasegawa '168; col. 6, lines 54-56 of Hasegawa '511. In addition, none of the references teach or suggest selecting a delay time is selected from delay time information according to input and output terminal logical state transitions of a circuit, as recited in claims 3 and 4. Since none of the references teach or suggest these features of claims 3 and 4, Applicant

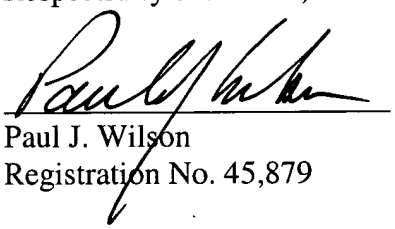
submits that one of ordinary skill in the art would not have been motivated to combine the three references. Thus, Applicant believes that the Examiner cannot fulfill the motivation prong of a *prima facie* case of obviousness with respect to claims 3 and 4, as required by *In re Dembiczak* and *In re Zurko*.

Based on the foregoing reasons, Applicant believes that the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 fails to disclose all of the claimed elements as arranged in claims 3 and 4. Therefore, the combination of Blinne *et al.*, Hasegawa '168 and Hasegawa '511 clearly cannot render the present invention obvious as recited in claims 3 and 4. Thus, Applicant believes that claims 3 and 4 are in condition for allowance. Applicant respectfully requests that the Examiner withdraw the § 103(a) rejection of claims 3 and 4.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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